



*SSC2100 Series
Application Note (Rev.1.1)*



SANKEN ELECTRIC CO., LTD.
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1. General Description

The SSC2101 series are controller ICs intended to implement a DCM (Discontinuous Conduction Mode) interleaved PFC (Power Factor Correction) circuit.

Using the two-phase interleaved control incorporated in this IC, it is possible to achieve a low cost, high performance PFC system with low input / output ripple currents, low noises and few external components.

2. Features

Features and benefits include the followings:

- Interleaved Discontinuous Conduction Mode (DCM) Operation
 - Low Peak Current, Low Ripple Current and Low Noise for Medium-to-High Power Applications

- Voltage Mode Control
 - No auxiliary windings on inductors required because of the built-in arithmetic circuit, achieving simple PFC system

- Maximum ON Time: 15 μ s(TYP)

- Built-in Soft Start Function
 - Stress reduction on power devices at start-up

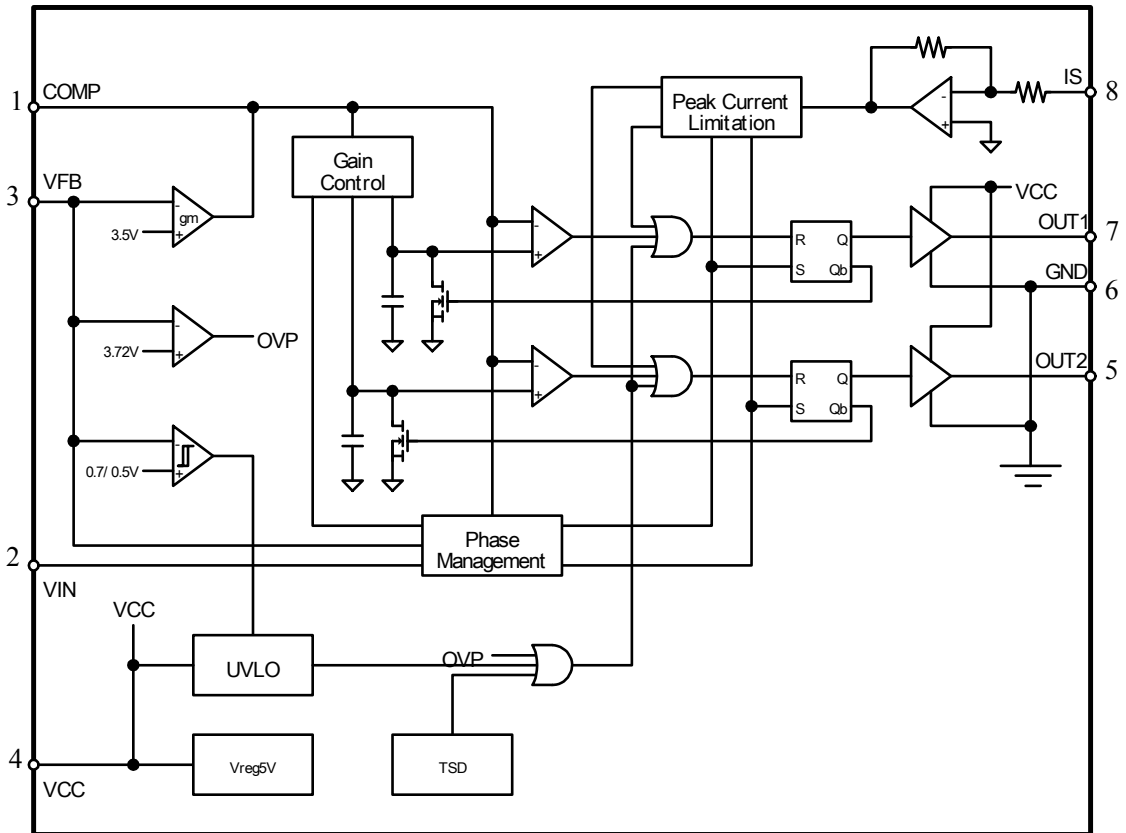
- Built-in High Speed Response (HSR)
 - Suppression of output voltage changes during dynamic load transient

- Error Amplifier Reference Voltage: 3.5V(TYP)

- Protection Functions
 - Soft Overvoltage Protection (SOVP) -----Output voltage decrease
 - Output Overvoltage Protection (OVP)-----Gate Drive off on pulse-by pulse basis, Auto-restart
 - Overcurrent Protection (OCP) -----Dual level OCP, Auto-restart
 - Output Open Loop Detection (OLD) -----Switching operation stop and transition to standby mode
 - Open Terminal Protection (OTP)-----Switching operation stop or Output voltage decrease during VFB terminal, VIN terminal or IS terminal is open
 - Thermal Shutdown (TSD)-----Auto-restart with hysteresis

3. Functional Block Diagram and Terminal List

Functional Block Diagram

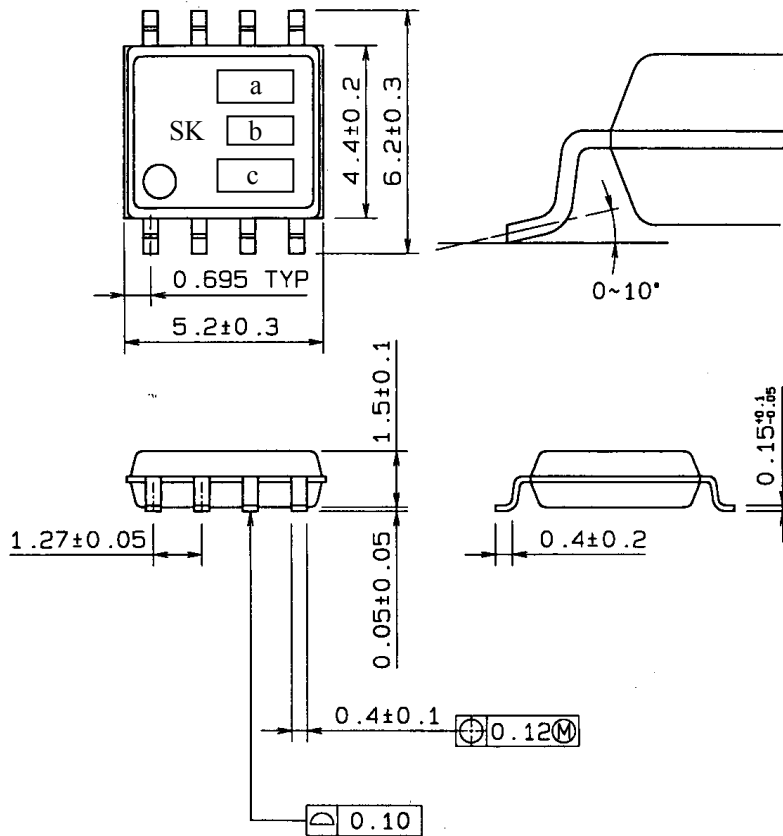


Terminal List

Terminal No	Symbol	Description	Functions
1	COMP	Error amplifier output terminal	Error amplifier output and phase compensation
2	VIN	Rectified mains voltage detection input terminal	Rectified input voltage detection
3	VFB	Feedback control terminal	Constant voltage control signal input / Overvoltage signal input / Open loop detection signal input
4	VCC	IC power supply terminal	Power supply for control circuit input
5	OUT2	Gate drive output 2 terminal	2nd Gate driver output
6	GND	Ground terminal	Ground
7	OUT1	Gate drive output 1 terminal	1st Gate driver output
8	IS	Current detection input terminal	Peak current detection signal input

4. Package Information

Standard 8 pin DIP package.



a. Type Number (Abbreviation)

SC2101

b. Lot Number

1st letter : The last digit of year

2nd letter : Month

1 to 9 for Jan. to Sept.

O for Oct.

N for Nov.

D for Dec.

3rd letter : Week

1st to 10th: 1

11th to 20th: 2

21st to 31st: 3

c. Sanken Registration Number

5. Electrical Characteristics

5.1 Absolute Maximum Ratings $T_a = 25^\circ\text{C}$, unless otherwise specified

Parameter	Terminal	Symbol	Ratings	Unit	Notes
VCC terminal voltage	4 – 6	V_{CC}	-0.3 to +30	A	-
COMP terminal voltage	1 – 6	V_{COMP}	-0.3 to +5.5	A	-
VFB terminal voltage	3 – 6	V_{FB}	-0.3 to +5.5	V	-
VFB terminal current	3 – 6	I_{FB}	-1 to +1	mA	-
VIN terminal voltage	2 – 6	V_{IN}	-0.3 to +5.5	V	-
VIN terminal current	2 – 6	I_{IN}	-1 to +1	mA	-
IS terminal voltage	8 – 6	V_{IS}	-16.0 to +5.5	V	-
IS terminal current	8 – 6	I_{IS}	-1.75 to +1	mA	-
OUT2 terminal voltage	5 – 6	V_{DR2}	-0.3 to +30	V	-
OUT1 terminal voltage	7 – 6	V_{DR1}	-0.3 to +30	V	-
Operating Frame Temperature	-	T_{FOP}	-40 to +85	$^\circ\text{C}$	-
Storage Temperature	-	T_{stg}	-40 to +125	$^\circ\text{C}$	-
Junction Temperature	-	T_j	-40 to +125	$^\circ\text{C}$	-

□ Current characteristics are defined based on IC as Sink: +, Source: -.

5.2 Electrical Characteristics in Control Part $T_a = 25^\circ\text{C}$, unless otherwise specified

Parameter	Terminal	Symbol	Ratings			Unit	Notes
			MIN	TYP	MAX		
Power Supply Start-up Operation							
VCC Operation start voltage	4 – 6	$V_{CC(ON)}$	10.8	11.6	12.4	V	—
VCC Operation stop voltage	4 – 6	$V_{CC(OFF)}$	9.8	10.6	11.4	V	—
VCC Undervoltage lockout hysteresis	4 – 6	$V_{CC(HYS)}$	0.8	1.0	1.2	V	—
VCC Circuit current in pre-operation	4 – 6	$I_{CC(OFF)}$	—	40	100	μA	—
VCC Circuit current in operation	4 – 6	$I_{CC(ON)}$	—	11.0	15.0	mA	—
VCC Circuit current during OVP	4 – 6	$I_{CC(OVP)}$	—	8.0	10.0	mA	—
VCC Circuit current during standby	4 – 6	$I_{CC(Standby)}$	—	100	200	μA	—
Oscillator Operation							
Max. ON time	7 – 6	t_{ONMAX}	14	15	16	μs	—
OUT1 to OUT2 ON time matching	5 – 6 7 – 6	t_{RATIO}	–5	0	5	%	—
OUT1 to OUT2 Phase difference	5 – 6 7 – 6	PHASE	170	180	190	deg	—
Protection Operation							
VFB Output open loop stop voltage	3 – 6	$V_{FB(OLDL)}$	0.46	0.50	0.54	V	—
VFB Output open loop start voltage	3 – 6	$V_{FB(OLDH)}$	0.64	0.70	0.76	V	—
VFB Output overvoltage protection voltage	3 – 6	$V_{FB(OVP)}$	3.64	3.72	3.80	V	—
VFB Output soft overvoltage protection voltage	3 – 6	$V_{FB(SOVP)}$	3.60	3.68	3.76	V	—
IS Lower overcurrent protection voltage	8 – 6	$V_{IS(OCPL)}$	–0.48	–0.42	–0.36	V	—
IS Upper overcurrent protection voltage	8 – 6	$V_{IS(OCPH)}$	–0.62	–0.55	–0.48	V	—
COMP Sink current during protection mode	1 – 6	$I_{COMP(SK)}$	80	100	120	μA	—
Upper thermal shutdown protection threshold	-	T_{JTSDH}	150	—	—	$^\circ\text{C}$	(Not tested)
Lower thermal shutdown protection threshold	-	T_{JTSDL}	140	—	—	$^\circ\text{C}$	
Thermal shutdown protection hysteresis	-	$T_{JTSDHYS}$	—	10	—	$^\circ\text{C}$	

□ Current characteristics are defined based on IC as Sink: +, Source: –.

Parameter	Terminal	Symbol	Ratings			Unit	Notes
			MIN	TYP	MAX		
Error AMP Operation							
VFB Error AMP reference voltage	3 – 6	$V_{FB(REF)}$	3.4	3.5	3.6	V	–
VFB Error AMP transconductance gain	–	gm_{EA}	80	100	120	μS	–
COMP Error AMP max. source current	1 – 6	$I_{COMP(SO)}$	–36	–30	–24	μA	–
COMP Error AMP max. output voltage	1 – 6	$V_{COMP(MAX)}$	4.00	4.12	4.25	V	–
VFB High speed response enable voltage	3 – 6	$V_{FB(HSR)enable}$	3.3	3.4	3.5	V	(Not tested)
VFB High speed response active voltage	3 – 6	$V_{FB(HSR)active}$	3.1	3.2	3.3	V	–
COMP High speed response source current	1 – 6	$I_{COMP(SOHSR)}$	–120	–100	–80	μA	–
VFB Input bias current	3 – 6	$I_{FB(bias)}$	–	–	1.5	μA	–
COMP Voltage during output open loop detection	1 – 6	$V_{COMP(OLD)}$	0.7	0.9	1.1	V	–
Drive Circuit							
OUT1,OUT2 Gate voltage (Low)	5 – 6 7 – 6	$V_{DR(L)}$	–	–	0.3	V	–
OUT1,OUT2 Gate voltage (High)	5 – 6 7 – 6	$V_{DR(H)}$	–	10.2	–	V	–
OUT1,OUT2 Rise time	5 – 6 7 – 6	t_r	–	70	–	ns	–
OUT1,OUT2 Fall time	5 – 6 7 – 6	t_f	–	35	–	ns	–
OUT1,OUT2 Peak source current	5 – 6 7 – 6	$I_{DR(SO)}$	–	–0.5	–	A	(Not tested)
OUT1,OUT2 Peak sink current	5 – 6 7 – 6	$I_{DR(SK)}$	–	0.5	–	A	

□ Current characteristics are defined based on IC as Sink: +, Source: –.

5.3 Package Thermal Characteristics $T_a = 25^\circ C$

Parameter	Terminal	Symbol	Ratings			Unit	Measurement Condition
			MIN	TYP	MAX		
Thermal resistance ※1	–	θ_{j-F}	–	65	85	$^\circ C/W$	Between junction and internal frame

※1 Internal frame temperature (T_F) is measured at the root of No.6 GND terminal.

6. Typical Application Circuit

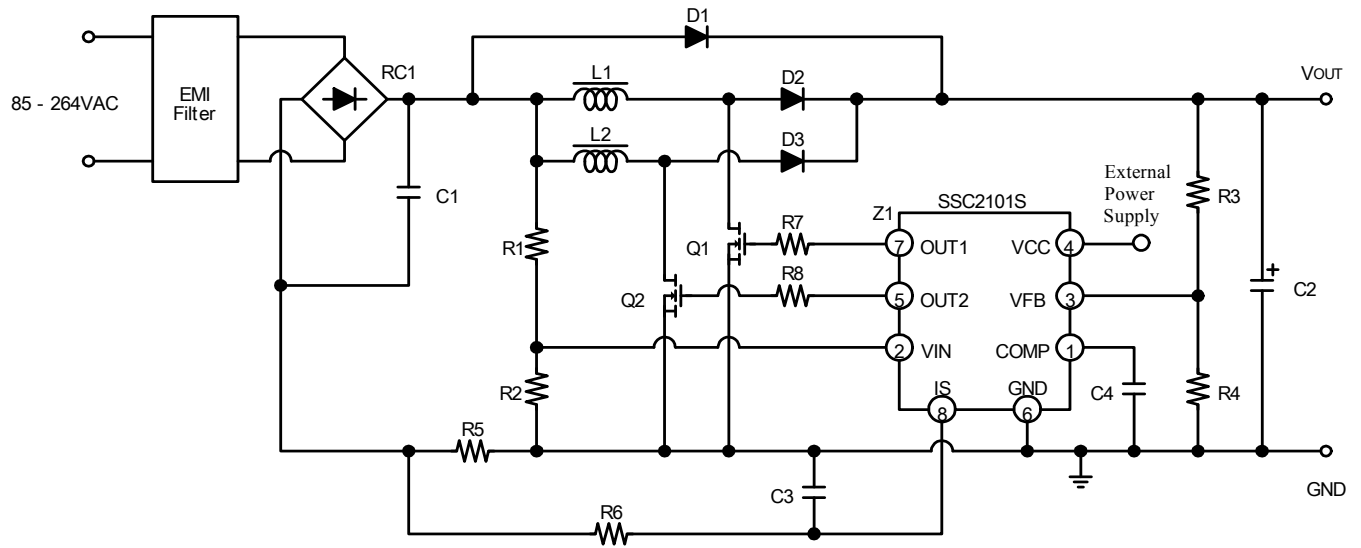


Figure 6 Typical application circuit example

7. Operational Descriptions of Interleaved Discontinuous Conduction Mode (DCM)

Discontinuous Conduction Mode (DCM) is well known as a technique that achieves low switching noises because the drain current increases from zero when a power MOSFET turns on, and is not steep shape waveforms as shown in figure 7-1. However, the usable power level of the single phase DCM is limited by the very high input / output ripple currents.

The two phase interleaved DCM incorporates two boost converters, and is able to cancel the input ripple currents and to reduce the output ripple currents due to the phase difference of 180° between two converters.

The interleaved DCM achieves a PFC system with lower switching noise and smaller input filter areas, compared with the single phase DCM. Because lower input / output ripple currents increase the filtering effect of EMI filters and reduce switching noises.

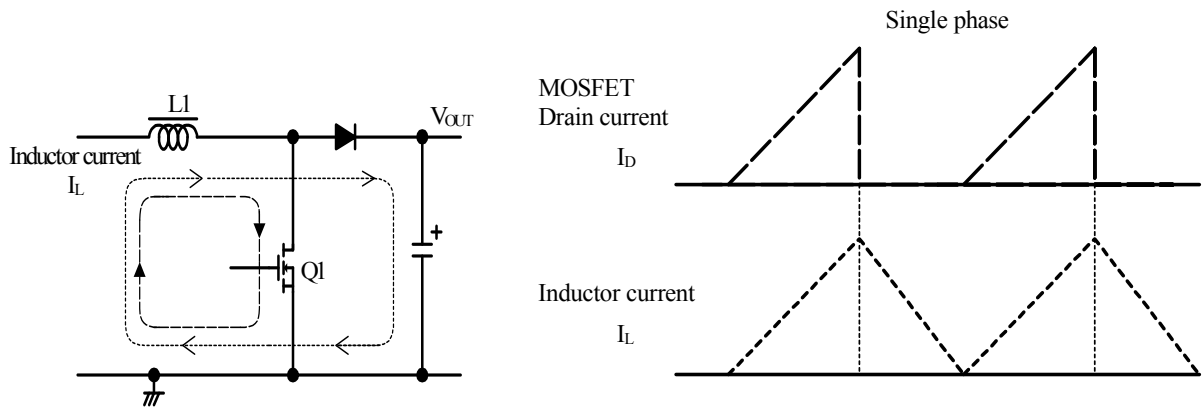


Figure 7-1 Current waveforms of single phase DCM

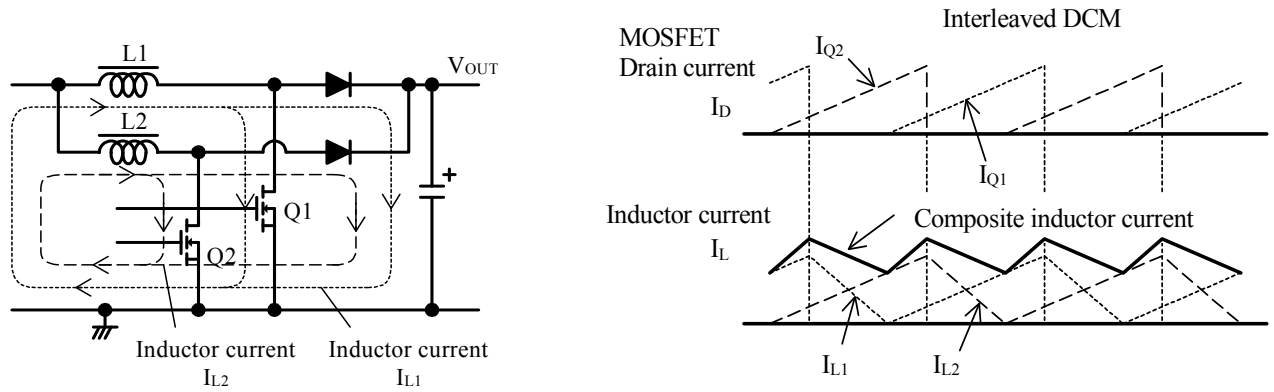


Figure 7-2 Current waveform of Interleaved DCM

8. Functional Descriptions

8.1 Startup Operation

The peripheral circuit around VCC terminal is shown in figure 8-1.

VCC terminal is the external power supply for the IC.

AC input voltage and the external voltage for VCC terminal are provided, and when VFB terminal voltage increases to $V_{FB(OLDH)} = 0.7V(TYP) \times$ or more and VCC terminal voltage increases to $V_{CC(ON)} = 11.6V(TYP)$ or more, the control circuit starts switching operation.

When VCC terminal voltage decreases to $V_{CC(OFF)} = 10.6V(TYP)$ or less, the control circuit stops switching operation by UVLO (Undervoltage lockout) circuit, and reverts to the standby mode before startup.

※ $V_{FB(OLDH)} = 0.7V(TYP)$ is equivalent to about 20% of the rated output voltage, V_{OUT} . One of the startup conditions is to be increased the input voltage to 20% or more of the rated output voltage, V_{OUT} .

When VFB terminal voltage decreases to $V_{FB(OLDL)} = 0.5V(TYP)$ or less, the control circuit stops switching operation and enters into the standby mode even if VCC terminal voltage increases to $V_{CC(ON)}$ or more.

As the control range of V_{CC} terminal is very wide, that is $V_{CC(OFF)} = 11.4V(MAX)$ to Maximum Rating = 30V(MAX), the wide input voltage range from the external power supply is available.

If the distance between the IC and C6 shown in figure 8-1 is lengthy, it is recommended to place C_f (a film capacitor of about 0.1 μF / 50V) close between VCC and GND terminals to prevent malfunctions caused by noise.

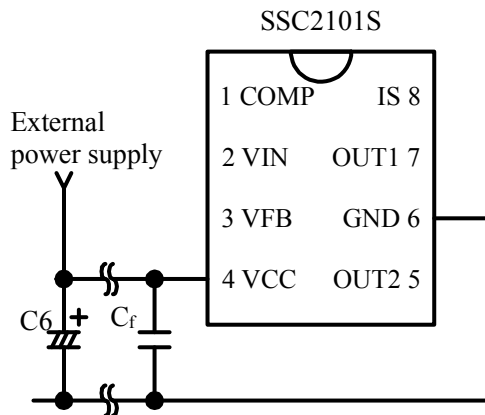


Figure 8-1 VCC peripheral circuit

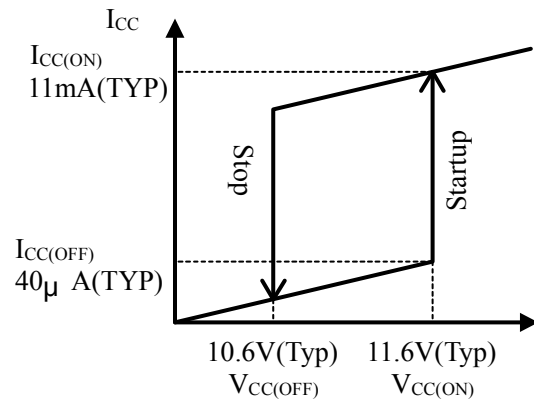


Figure 8-2 Relationship of V_{CC} and I_{CC} at startup and stop

8.2 Soft Start Function

When the input voltage increases to about 20% of the rated output voltage, V_{OUT} and V_{CC} terminal voltage increases to $V_{CC(ON)} = 11.6V(TYP)$, the soft start operation initiates at startup.

During soft start period, COMP terminal is charged by $I_{COMP(SO)} = -30\mu A$ as shown in figure 8-3, and thus the output power increases gradually to reduce stress on power devices.

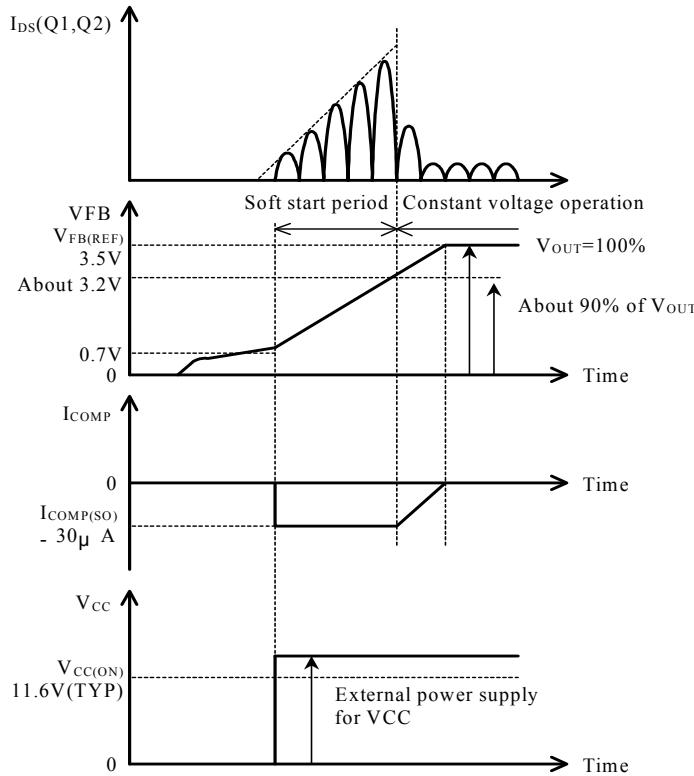


Figure 8-3 Soft start operation

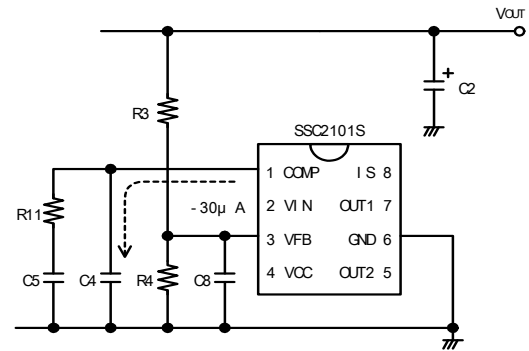


Figure 8-4 VFB, COMP peripheral circuit

8.3 Voltage Control Operation

The PFC circuit with a general single phase DCM is shown in figure8-5.

The PFC is composed of a boost inductor, $L1$, a switching device, $Q1$, a rectifier diode, $D2$, and an output capacitor, $C2$.

The control circuit detects $C2$ voltage and makes an error amp output signal, and this signal turns on $Q1$.

After $Q1$ is turned off, the energy stored in $L1$ is transferred to $C2$ through $D2$.

And when the control circuit detects the OFF timing from ZCD (Zero Current Detection) winding after all the energy stored in $L1$ is transferred to $C2$, and then $Q1$ is turned on. This operation is repeated

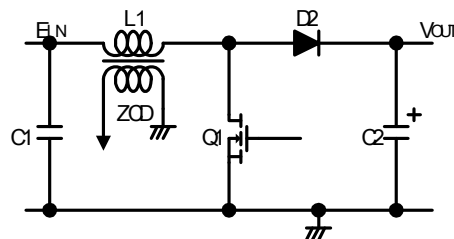


Figure 8-5 PFC circuit with a general single phase DCM

SSC2101S series detect the input voltage at V_{IN} terminal, the output voltage at V_{FB} terminal, and the phase compensation at $COMP$ terminal.

This IC makes the ON time (t_{ON}) and the OFF time (t_{OFF}) internally, and controls the output voltage by Voltage Mode Control method, and thus the PFC system with this IC needs no auxiliary winding detected zero crossings from inductor current, and achieves simple circuits with few external components.

In the boost PFC converter, the t_{ON} is a function of load power and the t_{OFF} is a function of the input voltage, E_{IN} , and the rated output voltage, V_{OUT} .

The relationship between t_{ON} and t_{OFF} is given by the following.

$$t_{OFF} > \frac{E_{IN}}{V_{OUT} - E_{IN}} \times t_{ON} \quad \text{-----(1)}$$

The typical relationship between V_{IN} and t_{ON} , on the condition that V_{COMP} is 4V, is shown below, where V_{IN} is V_{IN} terminal voltage, V_{COMP} is COMP terminal voltage.

The maximum $t_{ON(MAX)}$ is specified by $V_{IN}=0V$ and $V_{COMP}=4V$.

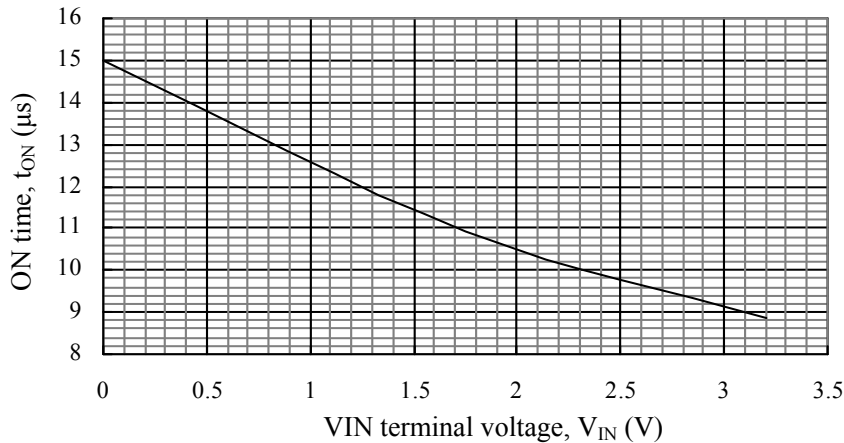


Figure 8-6 Typical relationship between V_{IN} and

V_{IN} terminal voltage detects the input voltage to calculate the internal t_{OFF} .

As shown in figure 8-7, the rectified input voltage is divided by R1 and R2, and input to V_{IN} terminal.

Because of the way V_{IN} terminal voltage and V_{FB} terminal voltage are used for internal calculation, the two dividers should be well matched, and thus R1, R2, C7 values of the input portion should be equal to R3, R4, C8 values of the output portion. R1 is recommended a high resistor in several hundreds k to several MΩ range and ±1% tolerance of anti-electronigration type, such as metal oxide film resistor. C8 is recommended a capacitor of about 0.1n to 10nF to reduce high frequency noises, if necessary.

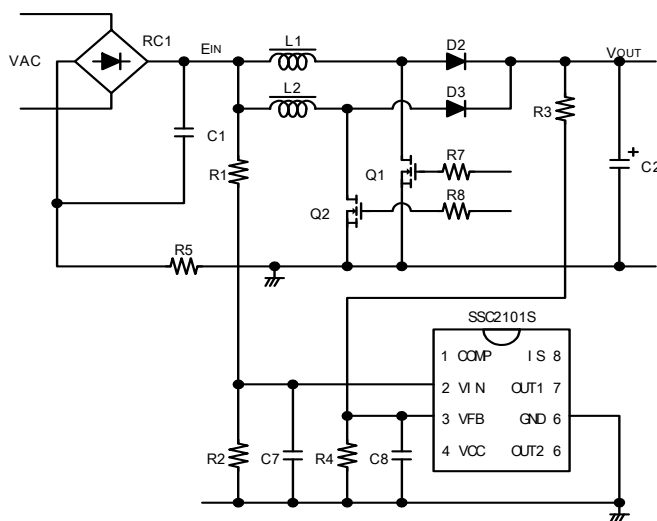


Figure 8-7 V_{IN} , V_{FB} peripheral circuit

8.4 High Speed Response Function (HSR)

The boost PFC is input the sinusoidal waveform of AC input voltage with commercial frequency, and the voltage control has the characteristic of responding to low frequency. As a result, the dynamic load response becomes slow, and may cause the output voltage to drop more easily.

HSR function is built-in to reduce variation of the output voltage under dynamic load change conditions.

As shown in Figure 8-8, when VFB terminal voltage increases to $V_{FB(HSR)enable} = 3.4V(TYP)$ or more, the control circuit enables HSR operation. After this, when VFB terminal voltage decreases to $V_{FB(HSR)active} = 3.2V(TYP)$ or less due to dynamic load change conditions or others, the control circuit starts HSR operation.

During this operation, COMP terminal is charged by $I_{VCOMP(SOHSR)} = -100\mu A(TYP)$ and the output power increases until COMP terminal voltage increases to 3.2V(TYP).

$V_{FB(HSR)active} = 3.2V(TYP)$ is equivalent to about 91.4% of the rated output voltage, V_{OUT} .

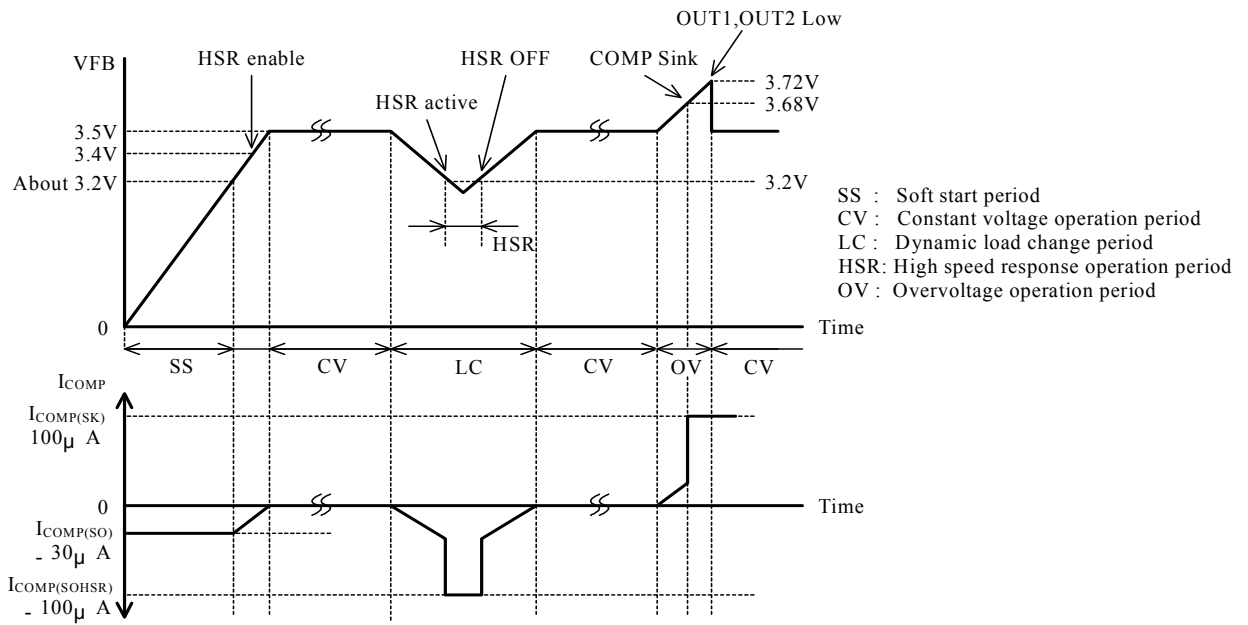


Figure 8-8 VFB terminal voltage waveform

8.5 Gate Drive

The OUT1 / OUT2 terminals directly drive an external power MOSFET as currents and voltages are set as follows.

- Peak Source Current / Peak Sink Current ----- $-0.5A(TYP) / 0.5A(TYP)$
- Gate Voltage (Low) / Gate Voltage (High) ----- $0.3V(MAX) / 10.2V(TYP)$

Resistors, R7, R8, R9 and R10 in figure 8-9 should be adjusted for actual operation because these values relate to the board layout patterns and power MOSFET capacities. The gate resistors, R7 and R8, are recommended in several to several tens of Ω range, and should be adjusted to reduce gate voltage ringing and EMI noise.

R9 and R10 help to prevent malfunctions caused by steep dV/dt during power MOSFET turns off.

The recommended values are in the 10k to 100k Ω range, and should be placed close to power MOSFET's gate and source terminals.

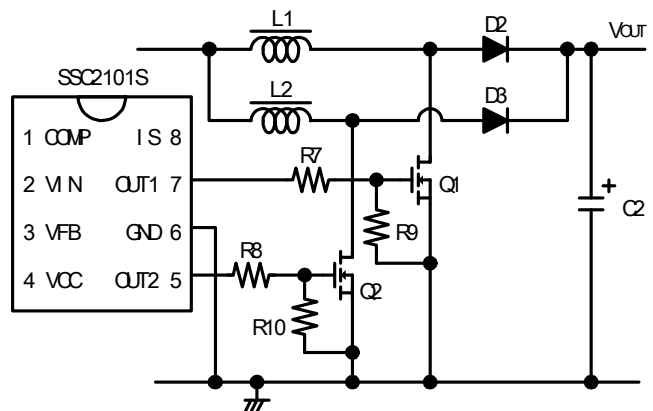


Figure 8-9 OUT1, OUT2 peripheral circuit

8.6 Error Amplifier Phase Compensation

COMP terminal is the output of the internal error amplifier. The error amplifier system consists of a transconductance amplifier and switched current sources that implement the enhanced response functions.

The phase compensation circuit is connected between COMP and GND terminals.

This response is set below 20 Hz to maintain power factor correction at standard commercial power frequencies of 50 or 60 Hz.

In figure 8-10, the phase compensation components, C4, C5 and R11, are recommended as follows, and may be adjusted to reduce ripple or to enhance transient load response at the output voltage.

- C4: 0.047 μ to 0.47 μ F
- C5: 0.47 μ to 10 μ F
- R11: 10k to 100k Ω

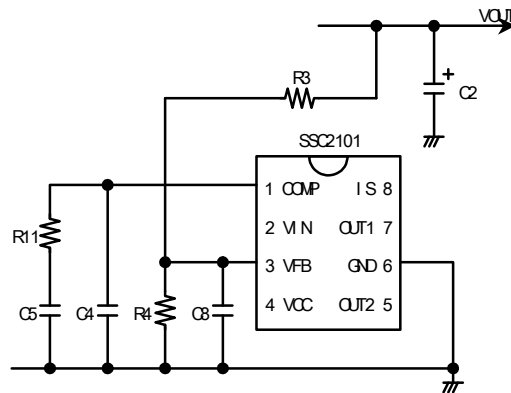


Figure 8-10 Phase compensation circuit
(COMP peripheral circuit)

8.7 Thermal Shutdown Protection (TSD)

When the temperature of the IC increases to $T_{jTSDH} = 150^{\circ}\text{C}$ (MIN) or more, the control circuit stops switching operation. Conversely, when that decreases to $T_{jTSDL} = 140^{\circ}\text{C}$ or less, the control circuit starts switching operation. The hysteresis of detection temperature, $T_{jTSDHYS}$, is 10°C (TYP).

8.8 Overcurrent Protection (OCP)

The inductor current of each inductor is detected by the detection resistor, R5, and is input to IS terminal.

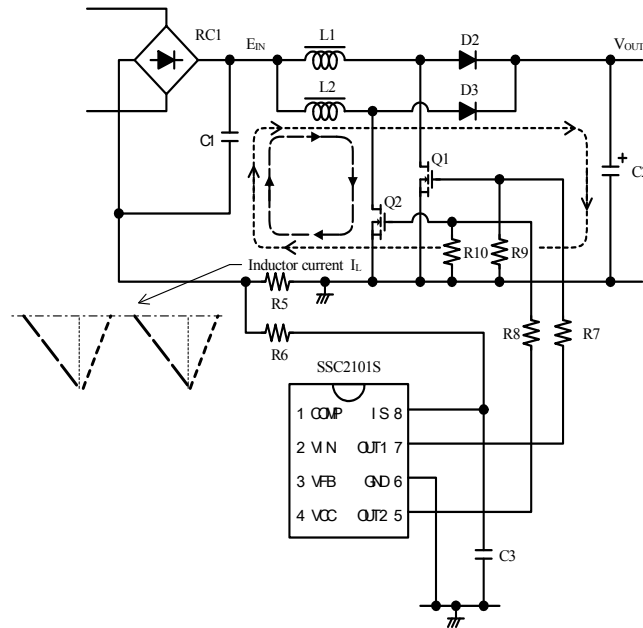


Figure 8-11 IS, OUT1, OUT2 peripheral circuit

The over-current protection has two steps as follows.

① IS Lower Overcurrent Protection --- $V_{IS(OCPL)}$

When the inductor current increases and IS terminal voltage decreases to $V_{IS(OCPL)} = -0.42V(TYP)$, the control circuit limits the output power by turning off one power MOSFET or two, according to the output state of both OUT1 and OUT2.

- When either OUT1 or OUT2 is high voltage, the output, which is set high, is set to low.
Figure 8-12 is an example. OUT2 is low and OUT1 is high, and IS terminal detects $|V_{IS(OCPL)}|$ or more during OUT1 is high (Q1 is ON). On this condition, OUT1 is set to low.

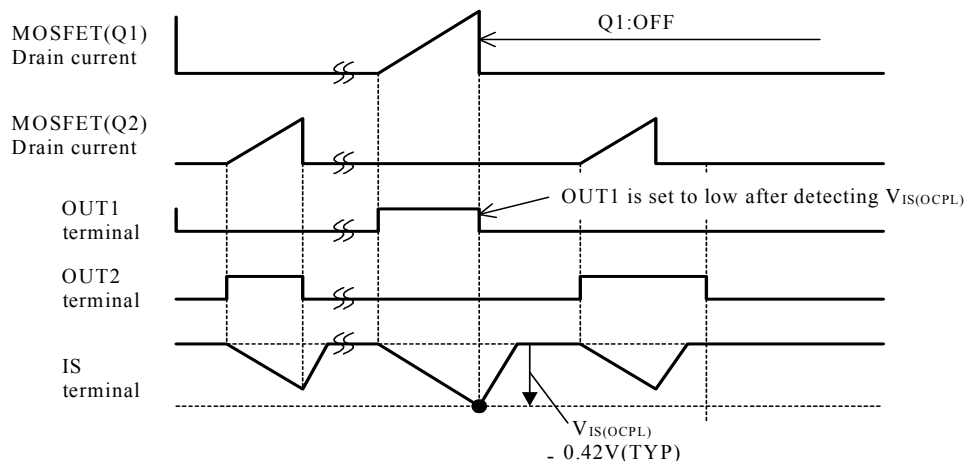


Figure 8-12 $V_{IS(OCPL)}$ operation waveform after OUT1 is set to high and OUT2 is set to low

- When both OUT1 and OUT2 are high voltage, the output which is set to high ahead is set to low.
Figure 8-13 is an example. Both OUT1 and OUT2 are high (Q1, Q2 are ON), and IS terminal detects $|V_{IS(OCPL)}|$ or more. On this condition, OUT1, which is set to high ahead, is set to low.

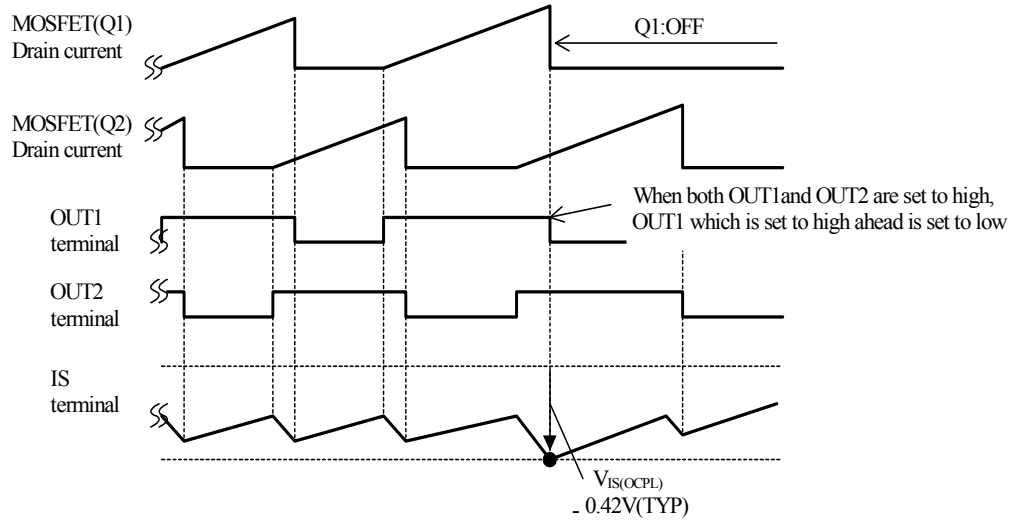


Figure 8-13 $V_{IS(OCPL)}$ operation waveform after both OUT1 and OUT2 are set to low

R5 in figure 8-11 should be adjusted on actual operation so that IS terminal voltage reaches $|V_{IS(OCPL)}|$ or more on the condition of minimum input voltage and peak load.

R6 is a limitation resistor, which limits IS terminal current against exceeding current, such as inrush currents, and is recommended 100Ω.

C3 is recommended a capacitor of about 0.1n to 10nF to reduce high frequency noises, if necessary.

②IS Upper Overcurrent Protection --- $V_{IS(OCPH)}$

When IS terminal voltage decreases to $V_{IS(OCPH)} = -0.55V(TYP)$ or less, the control circuit limits output power by turning off both power MOSFETs because both OUT1 and OUT2 are set to low on pulse-by-pulse basis.

This protection function operates on such abnormal conditions as the inductor is shorted or is saturated.

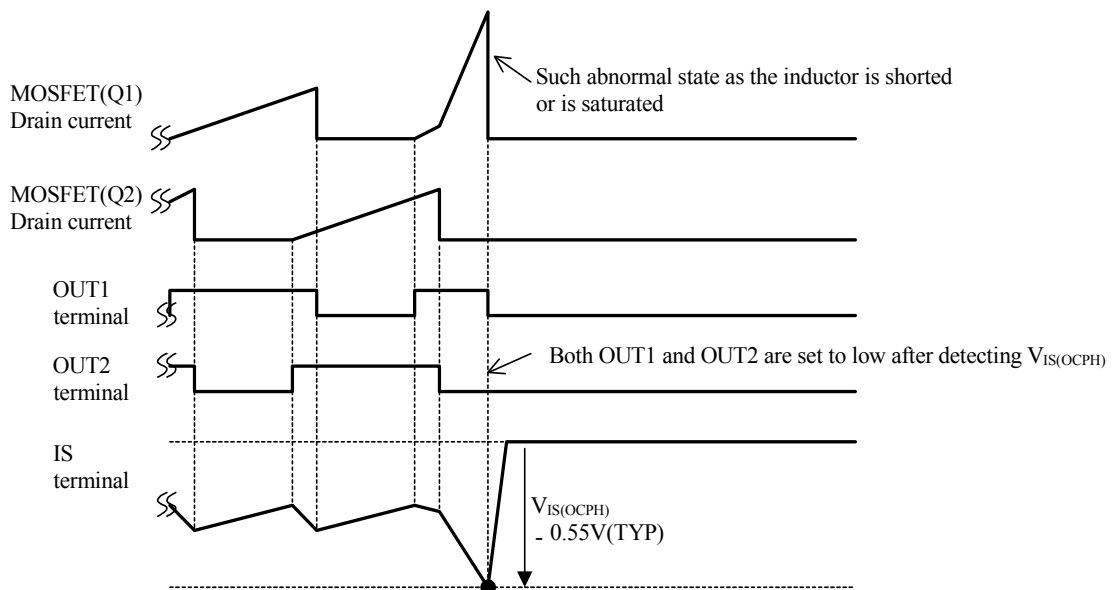


Figure 8-14 $V_{IS(OCPH)}$ operation waveform

8.9 Overvoltage Protection (OVP)

The overvoltage protection has two steps as follows. These operations are shown in figure 8-15.

①VFB Output Soft Overvoltage Protection --- $V_{FB(SOVP)}$

When VFB terminal voltage increases to $V_{FB(SOVP)}= 3.68V(TYP)$, Soft Overvoltage Protection is activated. And thus COMP terminal is discharged by $I_{COMP(SK)}= 100\mu A(TYP)$ and the output voltage is decreased. $V_{FB(SOVP)}= 3.68V(TYP)$ is equivalent to about 105% of the rated output voltage, V_{OUT} .

The output voltage, which operates Soft Overvoltage Protection, is calculated approximately as follows.

$$V_{OUT(SOVP)} = \frac{V_{OUT} \text{ (in normal operation)}}{V_{FB(REF)}} \times V_{FB(SOVP)} \quad \text{----- (2)}$$

where $V_{FB(REF)}$ is Error AMP reference voltage, 3.5V(TYP).

②VFB Output Overvoltage Protection --- $V_{FB(OVP)}$

When VFB terminal voltage increases to $V_{FB(OVP)}= 3.72V(TYP)$, both OUT1 and OUT2 are set to low on pulse-by-pulse basis and the output energy supply is stopped. After that, when VFB terminal voltage decreases to $V_{FB(SOVP)}$, the control circuit stops discharging from COMP terminal and reverts to switching operation.

The output voltage, which operates Overvoltage Protection, is calculated approximately as follows.

$$V_{OUT(OVP)} = \frac{V_{OUT} \text{ (in normal operation)}}{V_{FB(REF)}} \times V_{FB(OVP)} \quad \text{----- (3)}$$

R3 is recommended a high resistor in several hundreds k to several MΩ range and ±1% tolerance of anti-electronigration type, such as metal oxide film resistor.

C8 is recommended a capacitor of about 0.1n to 10nF to reduce high frequency noises, if necessary.

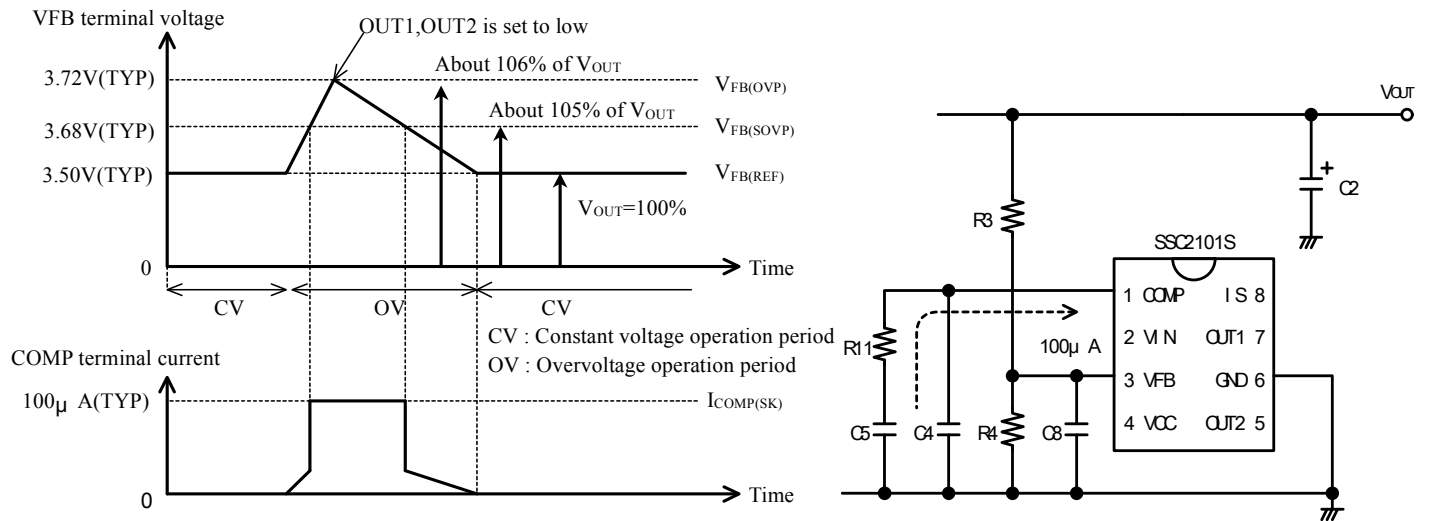


Figure 8-15 Overvoltage operation waveform

8.10 Open Loop Detection (OLD)

In case the output voltage detection resistor, R3, is open and VFB terminal voltage decreases to $V_{FB(OLDL)} = 0.5V(TYP)$ or less, the control circuit stops switching operation and enters into the standby mode.

$V_{FB(OLDL)} = 0.5V(TYP)$ is equivalent to about 14.3% of the rated output voltage, V_{OUT} .

When VFB terminal voltage increases to $V_{FB(OLDH)} = 0.7V(TYP)$ or more, the control circuit starts switching operation. $V_{FB(OLDH)} = 0.7V(TYP)$ is equivalent to about 20% of the rated output voltage, V_{OUT} .

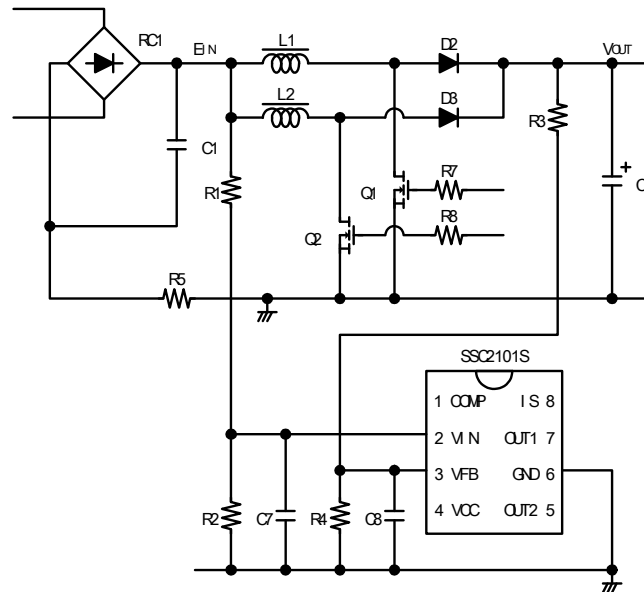


Figure 8-16 VFB peripheral circuit

8.11 Open Terminal Protection (OTP)

VFB, IS, VIN terminals have Open Terminal Protection internally.

- VFB Open Protection

VFB terminal is internally connected with a pull-up current source.

In case VFB terminal is open, VFB terminal voltage is pulled up to the internal supply voltage, the overvoltage protection is activated, and thus both OUT1 and OUT2 are set to low, the output voltage decreases.

- IS Open Protection

IS terminal is internally connected with a pull-up current source.

In case IS terminal is open, IS terminal voltage is pulled up to the internal supply voltage, the overcurrent protection is activated, and thus both OUT1 and OUT2 are set to low, the output power decreases.

- VIN Open Protection

VIN terminal is internally connected with a pull-up current source.

In case VIN terminal is open, VIN terminal voltage is pulled up to the internal supply voltage, the control circuit limits its operation, or stops.

9. Parameters Design

Symbols in this section are defined as follows.

- P_O : PFC Output power per phase (W)
- η : PFC Efficiency (%)
- t_{ON} : ON time (sec)
- V_{INRMS} : Input RMS voltage (V)
- V_{OUT} : PFC Output voltage (V)
- I_{INRMS} : Input RMS current (A)

The specifications of this design example are,

- AC input voltage: 85 to 264VAC
- Total output power of two phase Interleaved PFC total output power: 400W ($P_O = 200W$ for each phase)

① Output Voltage, V_{OUT} selection

The DC input voltage must always be lower than output voltage in a boost converter. Hence the rated output voltage, V_{OUT} , is set to at least 10V higher than the peak voltage of the commercial AC input voltage.

$$V_{OUT} \geq \sqrt{2} \times V_{INRMS} + 10(V) \quad \text{-----(4)}$$

(Ex.) $V_{OUT} \geq \sqrt{2} \times AC264V + 10V \cong 383(V)$, hence, V_{OUT} is set to DC390(V).

② Inductor Current

The waveform of the inductor current is triangular. The maximum peak current, $I_{LPEAK(MAX)}$, running through each inductor is calculated as follows.

- Maximum Input Power, $P_{IN(MAX)}$

Defining the output power margin as K_{OM} and the inductor saturation margin as K_{LM} , $P_{IN(MAX)}$ is calculated as follows.

$$P_{IN(MAX)} = \frac{K_{OM} \times K_{LM} \times P_O}{\eta} (W) \quad \text{-----(5)}$$

where η depends on the ON-resistance, $R_{DS(ON)}$, of the power MOSFET and the forward voltage, V_F of the rectifier diode. η is generally in the range of 0.90 to 0.97.

K_{OM} , K_{LM} depend on the design margins. Generally K_{OM} is the range of 1.2 to 1.3, K_{LM} is the range of 1.2 to 1.3 as reference.

$$(Ex.) P_{IN(MAX)} = \frac{1.2 \times 1.2 \times 200W}{0.92} \cong 313(W)$$

where it is assumed that K_{OM} is 1.2, K_{LM} is 1.2, and η is 0.92.

- Single Phase Inductor Peak Current, $I_{LPEAK(MAX)}$

Defining the minimum input RMS voltage as $V_{INRMS(MIN)}$, $I_{LPEAK(MAX)}$ is calculated as follows.

$$I_{LPEAK(MAX)} = \frac{2\sqrt{2} \times P_{IN(MAX)}}{V_{INRMS(MIN)}} \quad \text{-----(6)}$$

$$(Ex.) I_{LPEAK(MAX)} = \frac{2\sqrt{2} \times 313W}{AC85V} \cong 10.4(A)$$

③ Inductance Value

The inductance for a single phase, L is calculated as follows.

$$L \geq \frac{\sqrt{2} \times V_{INRMS(MIN)} \times t_{ON(MAX)}}{I_{LPEAK(MAX)}} \text{ (H)} \quad \text{-----(7)}$$

where $t_{ON(MAX)}$ is determined by V_{IN} terminal voltage, $V_{IN}(V)$, in figure 9-1.

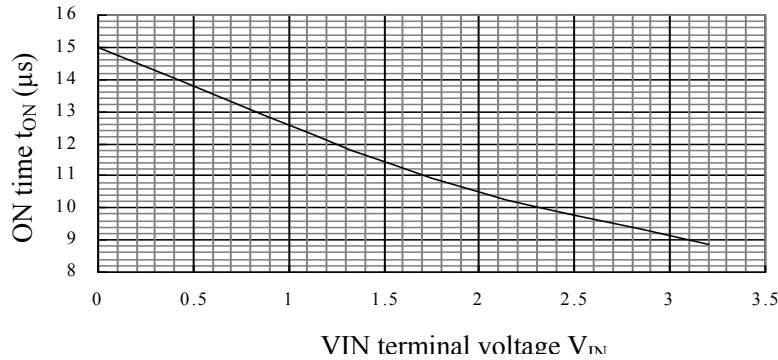


Figure 9-1 Typical relationship between V_{IN} terminal voltage and ON time

The values of R1 and R2 for V_{IN} terminal voltage detection should be equal to the values of R3 and R4 for V_{OUT} detection. Defining the rectified voltage as E_{IN} , V_{IN} terminal voltage, V_{IN} , is calculated as follows.

$$1 + \frac{R3}{R4} = \frac{V_{OUT}}{V_{FB(REF)}}, \text{ hence, } V_{IN} = \frac{E_{IN}}{V_{FB(REF)}}$$

(Ex.) V_{IN} terminal voltage, V_{IN} at 85VAC

$$1 + \frac{R3}{R4} = \frac{V_{OUT}}{V_{FB(REF)}} = \frac{390V}{3.5V} \cong 111.4$$

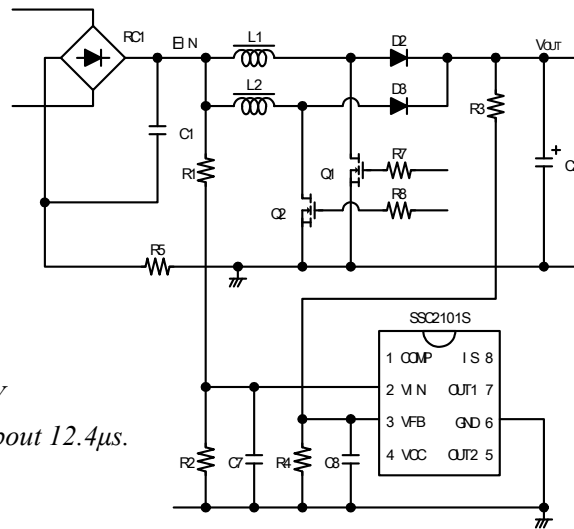
Hence,

$$V_{IN} \cong \frac{\sqrt{2} \times AC85V}{111.4} \cong 1.08(V)$$

$t_{ON(MAX)}$ is given by the point of $V_{IN}=1.08V$ in figure 9-1. From the graph, $t_{ON(MAX)}$ is about 12.4 μ s.

Thus,

$$L \geq \frac{\sqrt{2} \times AC85V \times 12.4\mu s}{10.4A} \cong 143(\mu H)$$



④ Inductor Turns

Defining the turns number of inductor as N, the effective area of inductor core as A_e (mm^2), and the maximum magnetic flux density as ΔB_{MAX} (mT), N is calculated as follows.

$$N = \frac{\sqrt{2} \times V_{INRMS(MIN)} \times t_{ON(MAX)}}{A_e \times \Delta B_{MAX}} \times 10^9 \text{ (turns)} \quad \text{-----(8)}$$

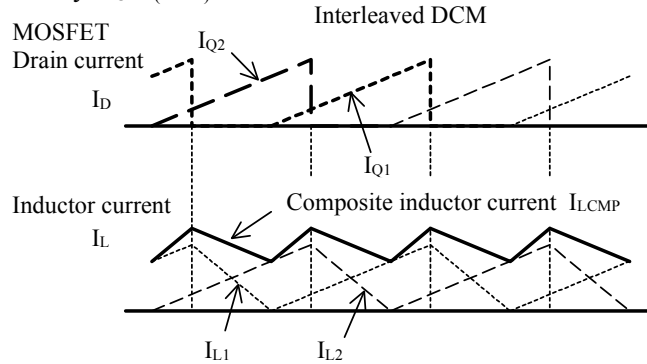
(Ex.) $N = \frac{\sqrt{2} \times AC85V \times 12.4\mu s}{102mm^2 \times 250mT} \times 10^9 \cong 58 \text{ (turns)}$

where it is assumed that A_e is $102mm^2$, ΔB_{MAX} is $250mT$.

⑤ Overcurrent Detection Resistor, R5

Overcurrent detection resistor, R5, detects the composite inductor current, I_{LCMP} , of both converters.

As the composite inductor current varies by ON-duty (D_{ON}), the coefficient defined as K_R is calculated from its D_{ON} , and R5 is calculated by $I_{LCMP(MAX)}$.



$$D_{ON(MAX)} = \frac{V_{OUT} - \sqrt{2} \times V_{INRMS(MIN)}}{V_{OUT}} \quad \text{----(9)}$$

(Ex.) $D_{ON(MAX)} = \frac{390V - \sqrt{2} \times AC\ 85V}{390V} \approx 0.69$

where K_R is given by the equation (10) when $D_{ON(MAX)}$ is 0.5 or more and by the equation (11) otherwise.

- When $D_{ON(MAX)} \geq 0.5$

$$K_R = 1 + \frac{D_{ON(MAX)} - 0.5}{D_{ON(MAX)}} \quad \text{----(10)}$$

(Ex.) $K_R = 1 + \frac{0.69 - 0.5}{0.69} \approx 1.28$

- When $D_{ON(MAX)} < 0.5$

$$K_R = 1 + \frac{0.5 - D_{ON(MAX)}}{1 - D_{ON(MAX)}} \quad \text{----(11)}$$

Thus, the composite inductor current, $I_{LCMP(MAX)}$ is calculated as follows.

$$I_{LCMP(MAX)} = K_R \times I_{LPEAK(MAX)}' \quad \text{----(12)}$$

where $I_{LPEAK(MAX)}'$ is calculated as follows.

$$I_{LPEAK(MAX)}' = \frac{2\sqrt{2} \times K_{OM} \times P_o}{\eta \times V_{INRMS(MIN)}}$$

(Ex.) $I_{LPEAK(MAX)}' = \frac{2\sqrt{2} \times 1.2 \times 200W}{0.92 \times AC\ 85V} \approx 8.7(A)$

Hence, $I_{LCMP(MAX)} = 1.28 \times 8.7A \approx 11.1(A)$

R5 is calculated from the peak current of the composite inductor current and the threshold voltage as follows.

$$R5 \leq \frac{|V_{IS(OCPL)}|}{I_{LCMP(MAX)}} (\Omega) \quad \text{----(13)}$$

(Ex.) $R5 \leq \frac{|-0.42V(TYP)|}{11.1A} (\Omega) \approx 0.038(\Omega)$

10. Design Notes

10.1 External Components

Take care to use properly rated, including derating as necessary, and proper type of components.

Refer to the parts number in Figure 10-2.

- Electrolytic capacitor, C2 :
Apply proper derating to ripple current, voltage, and temperature rise. Use of high ripple current and low impedance types, designed for switch mode power supplies, is recommended.
- Inductors, L1, L2 :
Apply proper derating against temperature rises by core and copper loss, for inductor L1, L2.
- Current detection resistor, R5 :
A high frequency switching current flows to R5, and may cause poor operation if a high inductance resistor is used. Choose a low inductance and surge-proof type.
- Higher resistors applied high voltage :
Choose a type, such as metal oxide film, that is not susceptible to degradation by electromigration, or by electrolytic corrosion or oxidation of the resistive material for high resistors applied high voltage.
- Bypass diode, D1 :
Choose a surge-current-proof type diode for D1, which is a bypass diode to protect D2, D3 against exceeding current such as inrush currents.
- Rectifiers D2, D3 :
Choose an ultra-high-speed type diode with short t_{rr} (reverse recovery time) for D2, D3 to reduce noise and power loss.
- Bypass diode and rectifier diodes for PFC :
As Sanken Electric has many lineups for bypass diodes and rectifiers for PFC application, please inquire of Sanken Electric Sales Department about them.

10.2 Pattern Design

PCB circuit trace design and component layout affect proper functioning during operation, EMI noise, and power dissipation.

Therefore, where high frequency current traces form a loop, as in Figure 10-1, wide, short patterns and small circuit loops are important to reduce line impedance. In addition, local GND and earth ground traces affect radiated EMI noise, and the same measures should be taken into account.

Switching mode power supplies consist of current traces with high frequency and high voltage, and then trace design and component layouts should be done to comply with all safety guidelines.

Furthermore, in the case where MOSFETs are being used as the switching device, take into account the positive thermal coefficient of $R_{DS(ON)}$ when preparing a thermal design.

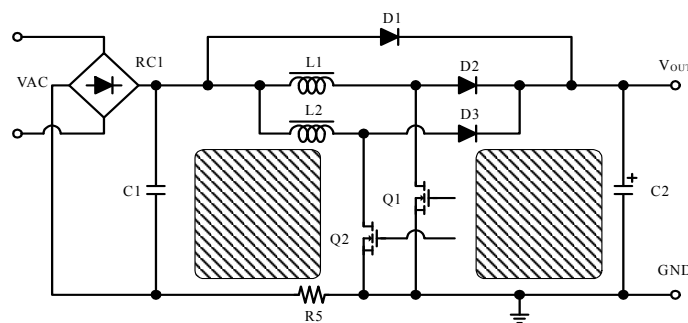


Figure 10-1 High Frequency Current Loop

Figure 10-2 shows the example of peripheral circuit connection.

- Avoid parallel patterns about control system patterns and main circuit patterns, so as not to be interfered by crosstalk noise.
- Connect GND terminal pattern to the root of R5 with shorter dedicated pattern, so as to reduce common impedance by separating the control system ground from main circuit ground, and connect R6 pattern also to the root of R5 with a dedicated pattern,
- Connect peripheral components to the IC with shorter patterns.
- Place C_f (a film capacitor in $0.1\mu\text{F}$ to $1\mu\text{F}$ /50V) between VCC and GND terminals, if the distance between C_6 and the IC is lengthly.
- Place R9 between GATE and SOURCE terminals of Q1.
- Place R10 between GATE and SOURCE terminals of Q2

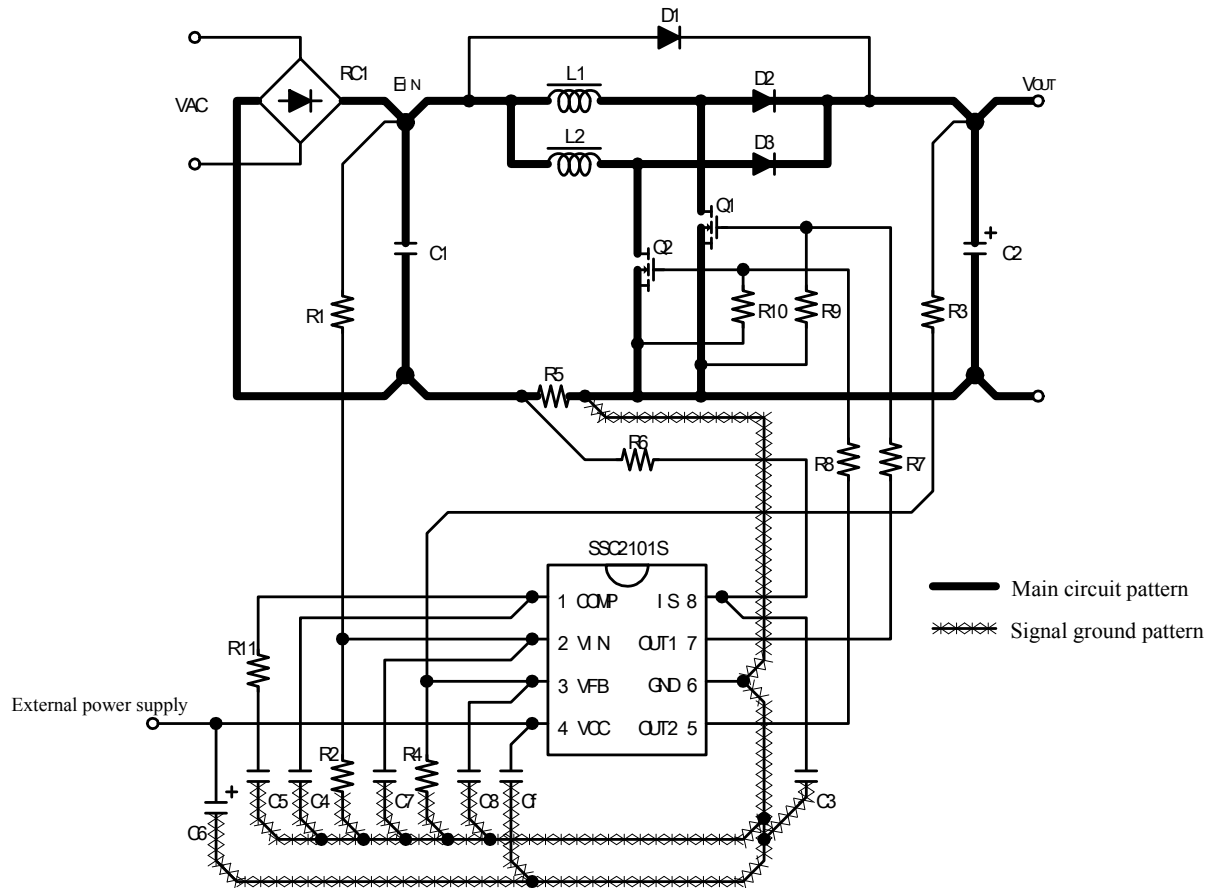


Figure 10-2 IC peripheral circuit connection example